

PCN Number: RC140304A (Revised 02/26/14) Notification Date*: February 19, 2014
See Below Correction in Blue Text

Title: Migration to Marketing Revision Level B of the AT91SAM7X512																		
Product Identification:																		
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Current Part Number</th> <th style="text-align: center;">New Part Number</th> </tr> </thead> <tbody> <tr> <td>AT91SAM7X512-AU</td> <td>AT91SAM7X512B-AU</td> </tr> <tr> <td>AT91SAM7X512-AU-999</td> <td>AT91SAM7X512B-AUR</td> </tr> <tr> <td>AT91SAM7X512-CU</td> <td>AT91SAM7X512B-CU</td> </tr> </tbody> </table>		Current Part Number	New Part Number	AT91SAM7X512-AU	AT91SAM7X512B-AU	AT91SAM7X512-AU-999	AT91SAM7X512B-AUR	AT91SAM7X512-CU	AT91SAM7X512B-CU							
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Reason for Change:	☐ Material / Composition ☒ Processing / Manufacturing ☒ Design / Firmware ☒ Datasheet	☐ Manufacturing Location ☐ Quality / Reliability ☐ Logistics ☐ Other:																
Change Description:																		
A complete list of differences between the marketing revision level (MRL) A and B can be found in chapter 41.2 of the AT91SAM7X series datasheet with Atmel document reference 6120K. The ChipID has been incremented to: AT91SAM7X512 Revision B chip ID is 0x275C 0A41 The Flash memory access time has been reduced as per the below table: <table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr> <th>Flash Wait State</th> <th>Read Operations</th> <th>Maximum Operating Frequency (MHz)</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1 cycle</td> <td>16</td> </tr> <tr> <td>1</td> <td>2 cycles</td> <td>32</td> </tr> <tr> <td>2</td> <td>3 cycles</td> <td>48</td> </tr> <tr> <td>3</td> <td>4 cycles</td> <td>55</td> </tr> </tbody> </table> Samples are available in Atmel Sample Center: https://samples.atmel.com/scripts/samplecenter.dll?atmel?cmd=menu				Flash Wait State	Read Operations	Maximum Operating Frequency (MHz)	0	1 cycle	16	1	2 cycles	32	2	3 cycles	48	3	4 cycles	55
Flash Wait State	Read Operations	Maximum Operating Frequency (MHz)																
0	1 cycle	16																
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Identification Method to Distinguish Change:																		
Marketing Revision Level (MRL) has been incremented on the top side marking to B .																		
Qualification Data:	☒ Available	☐ Will be available (mm/dd/yr):	☐ Not Applicable															
Samples:	☒ Available	☐ Will be available (mm/dd/yr):	☐ Not Applicable															
Quantifiable Impact on Quality & Reliability:																		
None																		

Forecasted Availability Date: February 20, 2014

Last Time Buy Date: May 20, 2014

Last Ship Date: February 20, 2015

**All orders placed after the notification date are non-cancellable and non-returnable (NCNR).*

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