



Product Change Notification / SYST-07EMYR287

Date:

08-Jan-2021

Product Category:

32-bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

Data Sheet - SAM D5X/E5X Family Datasheet Document Revision

Affected CPNs:

[SYST-07EMYR287_Affected_CPN_01082021.pdf](#)

[SYST-07EMYR287_Affected_CPN_01082021.csv](#)

Notification Text:

SYST-07EMYR287

Microchip has released a new Product Documents for the SAM D5X/E5X Family Datasheet of devices. If you are using one of these devices please read the document located at [SAM D5X/E5X Family Datasheet](#).

Notification Status: Final

Description of Change:

- 1) General: Along with the updates listed below, numerous typographical and minor editorial updates were made to this document.
- 2) Features: Updated Memories to show proper nomenclature for SmartEEPROM.
- 3) Configuration Summary: Updated Table 1-2 with new I2S specs for SAME51G18 and SAME51G19.
- 4) I/O Multiplexing and Considerations: Updated Table 6-34 GPIO Clusters, removed erroneous GPIO designations for the 100 pin package.

5) Memories: Updated Table 9-4 for bit position 75:64.

6) CMCC: Removed erroneous bitfields from the TYPE Register.

7) DSU:

- Updated SmartEEPROM nomenclature in Chip Erase

- Updated references to SmartEEPROM in Table 12-3 of 32-bit Cyclic Redundancy Check CRC32

- Updates table 12-6 in System Services Availability when Accessed Externally and Device is Protected with proper verbiage for SmartEEPROM

- Updated ENTRY0 and ENTRY1 registers with correct numbering

8) Clock System: Updated the Clock Request Routing Diagram in On Demand Clock Requests.

9) GCLK: Updated the GENCTRLn register with a new bitfield length for the SRC bit, and added new data to the end of table 14-4 Generator Clock Source Selection.

10) MCLK:

- Updated the table in Peripheral Clock Masking with new values for the ADC, NVMCTRL, and removed a reference to the PTC

- Updated the bitfield numbering and reset values in the following registers:

 - AHBMASK

 - APBCMASK

11) PM:

- Updated figure 18-2 in Sleepwalking

- Updated the register offset for the PWSAKDLY Register

12) SUPC: Removed an erroneous BOD12 reference from Enabling, Disabling, and Resetting.

13) RTC: Updated the COUNT32 Register with a new note.

14) DMAC: Updated the following registers with new bitfield verbiage:

- BASEADDR

- WRBADDR

- SRCADDR

- DSTADDR

15) GMAC:

- Updated the following registers with new bitfield information for bit 27:

- ISR

- IER

- IDR

- IMR

- Updated the TPB1ADR bit in the TPSF Register

- Updated the RPB1ADR bit in the RPSF Register

- Added the TPFCEP Register

- Renamed the bitfield in the TLPITI Register from RLPITI to TLPITI

16) NVMCTRL

- Updated verbiage for SmartEEPROM throughout the entire chapter

- Corrected typographical errors in Safe Flash Update Using Dual Banks

- Updated the CELCK Description in the table for the CMD bit in the CTRLB Register

17) ICM: Updated the Functional Description Overview topic with new verbiage for the end of list marker and WRAP bit setting.

18) OSCCTRL: Updated references for the SWBCK bit to the SWBEN bit in the Clock Switch section of Clock Failure Detection Operation.

19) OSC32KCTRL:

- Added a new note to 32 kHz Ultra Low-Power Internal Oscillator (OSCULP32K) Operation, and removed erroneous text references to the CALIB bit

- Updated the OSCULP32K Register with the removal of the erroneous CALIB bit, and converted it to a Reserved bit

20) EVSYS:

- Updated the following registers with new bitfield numbering:

- CHANNEL

- USERM

21) PORT: Updated the bitfield numbering for the PORTEIx, EVACTx, and PIDx bits in the EVCTRL Register.

22) SERCOM I2C:

- Corrected references for the LOWTOUTEN bit in Initialization

- Updated the CTRLA (Slave) Register with corrections to the name for the LOWTOUTEN bit
- Added a new LENERR bit to the STATUS (Slave) Register
- Updated the CTRLA (Master) Register with corrections to the name for the LOWTOUTEN bit

23) QSPI:

- Updated Serial Clock Phase and Polarity with new values for the Capture SCK Edge column in table 37-2
- Added a new note to QSPI Serial Memory Mode
- Updated the bitfield Access for the ENABLE bit in the CTRLA Register

24) USB: The STATUS (Device Registers - Common) was updated with new bitfield data.

25) CAN: Updates were made to the following Registers for bitfield naming, numbering, and typographical corrections:

- MRCFG
- ILE
- NDAT1
- NDAT2
- TXBRP
- TXBAR
- TXBCR
- TXBTO
- TXBCF
- TXBTIE
- TXBCIE
- TXEFS

26) SDHC:

- Removed erroneous Asynchronicity text in Clocks
- Updated the MAXBLKL bitfield with proper numbering in the CA0R Register
- Updated the PVR Register with the addition of the DRVSEL bitfield

27) CCL:

- Updated the Block Diagram to properly display only one layer
- Updated Signal Description with new Pin names
- Updated the LUTCTRL Register name

28) ADC: Removed erroneous RBSSW bitfield from the SYNCBUSY Register.

29) TC: Updated the Note in Capture Operations.

30) TCC:

- Updated the Block Diagram to display six Compare/Capture units
- Updated Principle of Operation to state six compare/Capture channels instead of four
- Updated the following Registers:
 - CTRLA with a new bit numbering for the CPTENx bitfield
 - EVCTRL with a new bit numbering for the MCEOx and MCEIx bitfields
 - The following registers have updates made to the MCx bitfields:
 - INTENCLR
 - INTENSET
 - INTFLAG
 - STATUS with a new bitfield numbering for CMPx and CCBUFVx

31) PCC:

- Removed erroneous text for transfer status signals from Principle of Operation
- Updated the text for line item number five in With DMAC
- Updated the following Registers with the removal of erroneous bitfields:
 - IER
 - IDR
 - IMR
 - ISR

32) PDEC: Added a new section to the chapter titled Secure Decoder Detection.

33) Electrical Characteristics at 85°C:

- Added a new note to I/O Pin Characteristics
 - Removed erroneous BIASREFBUF references from the Power Consumption table in Analog-to-Digital Converter (ADC) Characteristics
 - Removed the BANDGAP reference from Table 54-34 in Voltage References
 - In Internal Ultra Low Power 32 kHz RC Oscillator (OSCULP32K) Characteristics an erroneous Calibration column was removed from table 54-49
- 34) Appendix A: Added a new Appendix section for ISELED Specifications.

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 08 Jan 2021

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

[SAM D5X/E5X Family Datasheet](#)

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