

CN19009B: RTG4 PLL Lock Stability Customer Notification

Second Addendum

April 17, 2020

Summary

CN19009B is an addendum to CN19009 and CN19009A regarding the issue of RTG4 PLL lock stability over temperature. This addendum provides a final update on the investigation and provides final status on workarounds. Microsemi has concluded the investigation of possible workarounds to completely mitigate the temperature dependence across the full military temperature operating range.

Description of Change

RTG4 PLLs can experience loss of lock at high temperature after being initialized, via device power-up or PLL reset, at cold temperature. Once loss of lock happens, the PLL lock can be recovered by issuing a reset to the PLL. The root cause of the PLL loss of lock has been identified. Please refer to CN19009 and CN19009A for a description of the issue and prior guidance on workarounds.

Application Impact

Please refer to CN19009 and CN19009B for a description on the application impact.

In addition to the previously announced workarounds (Options 1A, 1B, and 2A from CN19009 and CN19009B), Microsemi has added support in Option 2A for the Fabric DDR (FDDR) controller PLL (FPLL) and for the SerDes PLL in the XAUI and PCI Express physical coding sublayer (SPLL). For reference, Option 2A enhances the calibration of the single-thread PLLs in the Fabric clock conditioning circuit (CCC), FDDR and SerDes so that the VCO is provided with additional gain at reset, and is capable of maintaining lock throughout the entire military temperature operating range. Validation of the Enhanced PLL calibration sequence has been completed for the FDDR PLL and SerDes SPLL. Microsemi will release updated FDDR and SerDes configuration cores to generate enhanced CoreABC initialization microcode that applies the PLL calibration sequence during the subsystem initialization. The enhanced PLL calibration cores for FDDR PLLs and SerDes PLLs are included in the upcoming Libero SoC v12.4 software release, and must be integrated into existing designs for the enhanced calibration to be applied to FDDR PLL and SerDes SPLL. The SPLL update does not impact the current functionality and operation of the transmit PLL (TXPLL) and clock and data recovery PLL (CDRPLL) within the PMA block. With this update, all single thread RTG4 PLLs will have lock stability independent of junction temperature rise during operation, within datasheet limits.

Attempts to validate Option 2B have been terminated. Option 2B was intended to provide enhanced calibration for the CCC PLL in triple module redundant (TMR) mode. The internal reset logic of the TMR PLL interferes with our ability to force the reset of the individual PLLs. This cannot be solved without all-layer changes to the silicon, which in turn would require a full requalification. Microsemi does not plan to make these changes. Customers may choose to use the previously-described solutions—options 1A, 1B, and 2A, as appropriate. All work on option 2B has been suspended.

Action Required

Customers who intend to use FDDR or SERDES in XAUI or PCIe modes are recommended to update to Libero SoC v12.4, to have access to new CoreABC initialization microcode which allows for higher start-up gain in the VCO of the DDR memory controller and SerDes PLLs. Designs completed using Libero SoC v11.x can update to Libero SoC v11.9 SP6 (when available) to access PLL calibration for the RTG4 DDR Memory Controller and High-Speed Serial Interface cores. The following user guides should be reviewed depending on the DDR and SerDes core used in the design:

- [RTG4 DDR Memory Controller Configuration User Guide](#)
- [RTG4 DDR Memory Controller with Initialization Configuration User Guide](#)
- [RTG4 FPGA DDR Memory Controller \(UG0573\)](#)
- [RTG4 High-Speed Serial Interface \(PCIe, EPCS and XAUI\) Config. User Guide \(UG0591\)](#)
- [RTG4 High-Speed Serial Interface \(EPCS and XAUI\) User Guide \(UG0592\)](#)

- [RTG4 High-Speed Serial Interface \(EPCS and XAUI\) with Initialization Configuration User's Guide \(UG0619\)](#)
- [RTG4 High-Speed Serial Interfaces User Guide \(UG0567\)](#)

Products Affected

The following table lists the affected products.

Microsemi Part Number	DLA SMD Number
RT4G150-CG1657B	5962-1620801QXF
RT4G150-1CG1657B	5962-1620802QXF
RT4G150-LG1657B	5962-1620803QZC
RT4G150-1LG1657B	5962-1620804QZC
RT4G150-CG1657E	5962-1620805QXF
RT4G150-1CG1657E	5962-1620806QXF
RT4G150-LG1657E	5962-1620807QZC
RT4G150-1LG1657E	5962-1620808QZC
RT4G150-CG1657V	5962-1620809VXF
RT4G150-1CG1657V	5962-1620810VXF
RT4G150-LG1657V	5962-1620811VZC
RT4G150-1LG1657V	5962-1620812VZC
RT4G150-CQ352B	5962-1620813QYC
RT4G150-1CQ352B	5962-1620814QYC
RT4G150L-CG1657B	5962-1620815QXF
RT4G150L-LG1657B	5962-1620816QZC
RT4G150L-CQ352B	5962-1620817QYC
RT4G150L-CG1657E	5962-1620818QXF
RT4G150L-LG1657E	5962-1620819QZC
RT4G150L-CG1657V	5962-1620820VXF
RT4G150L-LG1657V	5962-1620821VZC
RT4G150-1CB1657PROTO	
RT4G150-1CG1657PROTO	
RT4G150-1CQ352PROTO	
RT4G150-1LG1657PROTO	
RT4G150-CB1657PROTO	
RT4G150-CG1657PROTO	
RT4G150-CQ352PROTO	
RT4G150-LG1657PROTO	
RT4G150-1CG1657R	
RT4G150-1CQ352R	
RT4G150-1LG1657R	
RT4G150-CG1657R	
RT4G150-CQ352R	
RT4G150-LG1657R	

Microsemi Part Number	DLA SMD Number
RT4G150-1CG1657M	
RT4G150-1CQ352M	
RT4G150-1LG1657M	
RT4G150-CG1657M	
RT4G150-CQ352M	
RT4G150-LG1657M	
RT4G150-FCG1657M	
RT4G150-1FCG1657M	
RT4G150-FCG1657ES	
RT4G150-1FCG1657ES	

Contact Information

If you have any questions about this subject, contact Microsemi Technical Support department by using the support portal at <https://soc.microsemi.com/Portal/Default.aspx>

Regards,

Microsemi Corporation

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**Microsemi**

2355 W. Chandler Blvd.
Chandler, AZ 85224 USA

Within the USA: +1 (480) 792-7200
Fax: +1 (480) 792-7277

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