

Microsemi Corporation

May 21, 2019

Customer Notification No: CN19010

Subject

Libero SoC Timing Change and IO Glitch Notification

CAN 19010.1 Clock Source Latency Calculation

Description of the Issue

Due to an error introduced in Libero SoC v11.7-SP1, when a clock source latency constraint is applied to a generated clock, an additional delay (= late – early) is incorrectly added to the net driven by the clock source and impacting the required time calculation. As a result, the clock source latency constraint is ignored on the generated clock. Up until Libero SoC v12.0, this constraint has been recommended as a way to capture clock jitter information and pass it on to be used by the static timing analysis tool, SmartTime, during its Max Delay Analysis.

Reason for Notification

Libero SoC v11.9 SP2 and beyond restores the correct value for the data required time calculation. This correction is also addressed in Libero SoC v12.0. The respective software release notes include a reference to this change. In addition, starting with Libero SoC v12.0, jitter can also be modeled using simple clock uncertainty constraints.

Application Impact

Starting with Libero SoC v11.7 SP1 to v11.9 SP1, a clock source latency constraint set on a generated clock to capture, for example, internal PLL output jitter may have shown no timing violations in SmartTime that a proper accounting for the jitter might have flagged. There is no timing risk issue for cases where the slack of the max delay path is greater than the total jitter window (late-to-early value). However, if such slack is less than the jitter window, there is a risk for a timing violation that the tool would have not flagged in the affected versions. See Table 283 in the SmartFusion2/IGLOO2 datasheet for jitter specifications.

Action Required

Re-run static timing analysis with SmartTime using Libero SoC v11.9 SP2 or later, if you are setting a clock source latency constraint on a generated clock and the margin you have is less than the constraint window (for example, jitter window).

CAN 19010.2 IO Glitches During Auto-Update

Description of Change

Auto-update is a method to automatically update the FPGA image on a power-up. If enabled, the system controller will check the design version of a bitstream in an external SPI flash and compare it to the programmed version. If the external bitstream is newer than the programmed bitstream, then the system controller will use the new bitstream to program the device. If auto-update is enabled, an auto-update action will occur. Under these conditions during device power-up or the de-assertion of DEVRST_N, an IO glitch will occur on banks 0, 1, and 2 of the the M2S005/010/025 or M2GL005/010/025 devices. If auto-update is not enabled, the glitch does not occur. The amplitude of the glitch correlates to the VDDI bank voltage level.

Reason for Notification

IO glitches on banks 0, 1, and 2 of the the M2S005/010/025 or M2GL005/010/025 devices during auto-update programming mode.

Application Impact

The IO glitch is a drive-high glitch with <10 ns duration. The glitch occurs before the FPGA user IOs are activated and the FPGA fabric comes out of reset. Note that DEVRST_N is not needed for proper device operation. DEVRST_N resets the system controller effectively causing a warm boot of the device. Users should always use a GPIO to perform a user design reset.

Workaround

- Utilize In-Application Programming (IAP) in place of auto-update.
- Move sensitive outputs to a non-glitch bank.

Contact Information

If you have further questions about this subject, contact Microsemi Technical Support department by using the support portal at <https://soc.microsemi.com/Portal/Default.aspx>

Regards,

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Affected Part Numbers

SmartFusion2 Leaded Parts	SmartFusion2 Lead-Free Parts	IGLOO2 Leaded Parts	IGLOO2 Lead-Free Parts
M2S005-TQ144	M2S005-TQG144	M2GL005-TQ144	M2GL005-TQG144
M2S010-TQ144	M2S010-TQG144	M2GL010-TQ144	M2GL010-TQG144
M2S005-VF256	M2S005-VFG256	M2GL005-VF256	M2GL005-VFG256
M2S010-VF256	M2S010-VFG256	M2GL010-VF256	M2GL010-VFG256
M2S025-VF256	M2S025-VFG256	M2GL025-VF256	M2GL025-VFG256
M2S025-FCS325	M2S025-FCSG325	M2GL025-FCS325	M2GL025-FCSG325
M2S005-VF400	M2S005-VFG400	M2GL005-VF400	M2GL005-VFG400
M2S010-VF400	M2S010-VFG400	M2GL010-VF400	M2GL010-VFG400
M2S025-VF400	M2S025-VFG400	M2GL025-VF400	M2GL025-VFG400
M2S005-FG484	M2S005-FGG484	M2GL005-FG484	M2GL005-FGG484
M2S010-FG484	M2S010-FGG484	M2GL010-FG484	M2GL010-FGG484
M2S025-FG484	M2S025-FGG484	M2GL025-FG484	M2GL025-FGG484
M2S010T-VF256	M2S010T-VFG256	M2GL010T-VF256	M2GL010T-VFG256
M2S025T-VF256	M2S025T-VFG256	M2GL025T-VF256	M2GL025T-VFG256
M2S025T-FCS325	M2S025T-FCSG325	M2GL025T-FCS325	M2GL025T-FCSG325
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M2S025T-VF400	M2S025T-VFG400	M2GL025T-VF400	M2GL025T-VFG400
M2S010T-FG484	M2S010T-FGG484	M2GL010T-FG484	M2GL010T-FGG484
M2S025T-FG484	M2S025T-FGG484	M2GL025T-FG484	M2GL025T-FGG484
M2S050T-FG484	M2S050T-FGG484	M2GL050T-FG484	M2GL050T-FGG484
M2S005S-TQ144	M2S005S-TQG144	M2GL005S-TQ144	M2GL005S-TQG144

SmartFusion2 Leaded Parts	SmartFusion2 Lead-Free Parts	IGLOO2 Leaded Parts	IGLOO2 Lead-Free Parts
M2S010S-TQ144	M2S010S-TQG144	M2GL010S-TQ144	M2GL010S-TQG144
M2S005S-VF256	M2S005S-VFG256	M2GL005S-VF256	M2GL005S-VFG256
M2S005S-VF400	M2S005S-VFG400	M2GL005S-VF400	M2GL005S-VFG400
M2S005S-FG484	M2S005S-FGG484	M2GL005S-FG484	M2GL005S-FGG484
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M2S005S-1FG484	M2S005S-1FGG484	M2GL005S-1FG484	M2GL005S-1FGG484
M2S010TS-1VF256	M2S010TS-1VFG256	M2GL010TS-1VF256	M2GL010TS-1VFG256

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M2S025TS-1VF256	M2S025TS-1VFG256	M2GL025TS-1VF256	M2GL025TS-1VFG256
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M2S025TS-1VF400	M2S025TS-1VFG400	M2GL025TS-1VF400	M2GL025TS-1VFG400
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SmartFusion2 Leaded Parts	SmartFusion2 Lead-Free Parts	IGLOO2 Leaded Parts	IGLOO2 Lead-Free Parts
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**Microsemi Headquarters**

One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

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One Enterprise, Aliso Viejo, CA 92656 USA
Within USA: +1 (800) 713-4113 Outside USA: +1 (949) 380-6100 Fax:
+1 (949) 215-4996 Email: AVO-sales.support@microsemi.com
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